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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,991	05/02/2001	Jason Seung-Min Kim	2100653-991140	5788

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EXAMINER	
MYERS, PAUL R	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/847,991	KIM ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 7/6/04 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicants arguments are not commemorate with the claims pending in the instant application. A true copy of the claims pending in the included with this action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 8-9, 11-13, 18-19, 21-22, 24-25 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by MacLellan et al (USPN 6,636,933; MacLellan).

As per claims 1,11, and 21, MacLellan discloses a computer system (100) having a multipath cross bar bus (crossbar 260), comprising: one or more processors (121); one or more resources (memory 220 or disk drives 140) capable of being shared by the one or more processors; and a resource controller (controller 260) and bus that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous accesses; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2).

As per claims 2 and 12, MacLellan discloses memory resources (plural global memory boards 220; col. 12, lines 41+; Fig. 8; col. 14, lines 12+ to col. 15, lines 1+); memory controller (logic sections e.g. 5010; col. 18, lines 42-55);

As per claims 3, 13 and 22, MacLellan discloses crossbar switches 5004 (col. 18, lines 5+); and resource arbitration controller (fig. 10; col. 19, lines 11+; col. 23, lines 26+);

As per claims 8, 18 and 24, MacLellan discloses a plurality of peripheral resources (plural disks drives 140); and peripheral controller (switch controller 260) wherein the controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2).

As per claims 9, 19 and 25, MacLellan discloses crossbar switches 5004 (col. 18, lines 5+); and resource arbitration controller (fig. 10; col. 19, lines 11+; col. 23, lines 26+);

As per claim 27, MacLellan discloses a computer system (100; fig. 1) comprising: a first processor (121_1); a second processor (121_2); a multipath memory controller (controller 260) having a first bus that is capable of connecting the first processor to a set of memory resources and a second bus that is capable of connecting the second processor to the same set of memory resources wherein the first and second processors are capable of simultaneously accessing different memory resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2); a multipath peripheral controller (controller 260) having a first bus that is capable of connecting the first processor to a set of peripheral resources (disk drives) and a second bus that is capable of connecting the second processor to the same set of peripheral resources (disk drives) wherein the first and second processors are capable of simultaneously accessing different peripheral resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2).

4. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Srini (USPN 5,053,942).

As per claim 1, Srini discloses a computer system (e.g. Fig. 1) having a multipath cross bar bus (crossbar matrix 20), comprising: one or more processors (12); one or more resources (memory 22) capable of being shared by the one or more processors (12); and a resource controller (crossbar chip 10) and bus (26) that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (e.g. col. 8, lines 30-50).

As per claim 2, Srini discloses memory resources (plural memory modules 22; col. 4, lines 15+); memory controller (arbiter 18 and logic; col. 4, lines 41-51);

As per claim 3, Srini discloses crossbar switches 20; and resource arbitration controller (arbiter 18; col. 4, lines 41+)

5. Claims 1-3, 8-9, 11-13, 18-19, 21-22, 24-25 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Goodwin et al. (USPN 6,125,429; Goodwin).

As per claims 1, 11 and 24, Goodwin discloses a computer system (e.g. Fig. 1) having a multipath crossbar bus (crossbar 12), comprising: one or more processors (CPU0 to CPU3); one or more resources (memory M0-M3 or I/0 16) capable of being shared by the one or more processors (CPU0-CPU3); and a resource controller (arbitor 14) and bus that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (e.g. col. 2, lines 46-52; col. 4, lines 26-36; 49-62).

As per claims 2, 8, 12, 18 and 25, Goodwin discloses memory or peripheral resources (plural memory modules M0-M3; col. 4, lines 26+; or I/O 16); memory or peripheral controller (arbiter chip 14; col. 4, lines 61+);

As per claims 3, 9, 13 and 19, Goodwin discloses crossbar switches 12; and resource arbitration controller (arbiter 14; col. 4, lines 26+)

As per claim 21, Goodwin discloses an apparatus for controlling the access to one or more memory resources by one or more processors, the controller comprising a memory resource controller (arbitor 14) and bus (crossbar switch) that is connected to each memory resource and to each processor so wherein the memory resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more memory resources (col. 2, lines 45-52; col. 4, lines 26-36; 49-62).

As per claim 22, Goodwin discloses crossbar switches 12; and resource arbitration controller (arbiter 14; col. 4, lines 26+)

As per claim 27, Goodwin discloses a computer system (10; fig. 1) comprising: a first processor (20); a second processor (22); a multipath memory controller (arbitor 14 and x-bar switch 12) having a first bus that is capable of connecting the first processor to a set of memory resources and a second bus that is capable of connecting the second processor to the same set of memory resources wherein the first and second processors are capable of simultaneously accessing different memory resources (col. 2, lines 45-52; col. 4, lines 26-36; 49-62); a multipath peripheral controller (arbitor 14 and x-bar switch 12) having a first bus that is capable of connecting the first processor to a set of peipheral resources and a second bus that is capable of connecting the second processor to the same set of peripheral resources wherein the first and

second processors are capable of simultaneously accessing different peripheral resources (col. 2, lines 45-52; col. 4, lines 26-36; 49-62).

6. Claims 1-2, 11-12, 21 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiller et al. (USPN 5,081,575; Hiller).

As per claims 1, 11 and 24, Hiller discloses a computer system (e.g. Fig. 1) having a multipath crossbar bus (crossbar 6), comprising: one or more processors (PEs); one or more resources (PMEMs 8) capable of being shared by the one or more processors (PEs); and a resource controller (control section) and bus (crossbar bus) that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (e.g. col. 6, lines 55-57).

As per claims 2 and 12, Hiller discloses memory (PMEMs 8); memory controller (control section; col. 6, lines 55 et seq).

As per claim 21, Hiller discloses an apparatus for controlling the access to one or more memory resources (PMEMs) by one or more processors (PEs), the controller comprising a memory resource controller (control section; col. 6, lines 55 et seq) and bus (crossbar switch) that is connected to each memory resource and to each processor so wherein the memory resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more memory resources (col. 6, lines 55-57).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3-4, 13-14, 22-23 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable Hiller et al. (USPN 5,081,575; Hiller) in view of Goodwin et al. (USPN 6,125,429; Goodwin).

As per claims 3, 13, 23 and 25; Hiller discloses crossbar switch 6. However, Hiller does not teach an arbitration controller. Goodwin teaches that it is known to use a resource arbitration controller to resolve contentions or collisions in a computer system using a crossbar switch (col. 2, lines 30-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hiller and Goodwin as taught by Goodwin to include a resource arbitration controller in a crossbar switch type system such as that of Hiller to resolve the collisions and contentions particularly in bus systems such as that of Hiller with large numbers of data users (PEs) and resources (PMEMs) connected to them (col. 2, lines 55-67).

As per claims 4, 14, 23 and 26, Hiller teaches that the crossbar switch comprises multiplexer (col. 6, lines 57-64).

9. Claims 4-7, 10, 14-17, 20, 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable MacLellan et al (USPN 6,636,933; MacLellan) in view of Official Notice as evidenced by Hiller et al. (USPN 5,081,575; Hiller).

As per claims 4, 7, 10, 14, 17, 20, 23, and 26, MacLellan teaches all the limitations of the claimed invention including crossbar switch. However, MacLellan is silent as to the switch comprise multiplexer. Official Notice is taken that crossbar switch comprise a multiplexer is notoriously well known in the crossbar switch art at the time the invention was made such as evidenced by Hiller in that multiplexer is utilized in crossbar switch do perform actual switching of signal paths (bus) to connect pairs of processors and resources.

As per claims 5 and 15, MacLellan discloses a plurality of peripheral resources (plural disks drives 140); and peripheral controller (switch controller 260) wherein the controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2).

As per claims 6 and 16, MacLellan discloses crossbar switches 5004 (col. 18, lines 5+); and resource arbitration controller (fig. 10; col. 19, lines 11+; col. 23, lines 26+);

10. Claims 4-7, 10, 14-17, 20, 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodwin et al. (USPN 6,125,429; Goodwin) in view of Official Notice as evidenced by Hiller et al. (USPN 5,081,575; Hiller).

As per claims 4, 7, 10, 14, 17, 20, 23, and 26, Goodwin teaches all the limitations of the claimed invention including crossbar switch. However, Goodwin is silent as to the switch comprise multiplexer. Official Notice is taken that crossbar switch comprise a multiplexer is

notoriously well known in the crossbar switch art at the time the invention was made such as evidenced by Hiller in that multiplexer is utilized in crossbar switch do perform actual switching of signal paths (bus) to connect pairs of processors and resources.

As per claims 5 and 15, Goodwin discloses memory or peripheral resources (plural memory modules M0-M3; col. 4, lines 26+; or I/O 16); memory or peripheral controller (arbiter chip 14; col. 4, lines 61+);

As per claims 6 and 16, Goodwin discloses crossbar switches 12; and resource arbitration controller (arbiter 14; col. 4, lines 26+).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 703 305 9656. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703 305 4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRM
September 30, 2004

PAUL R. MYERS
PRIMARY EXAMINER